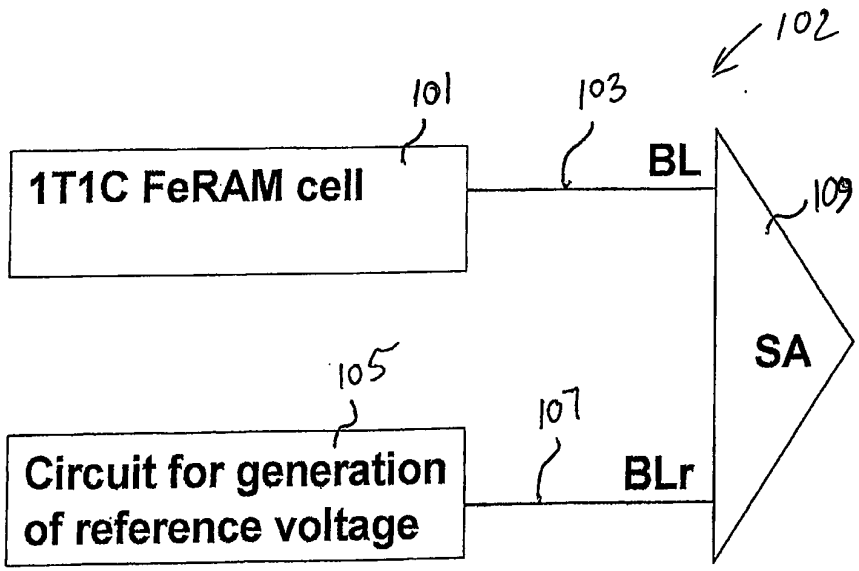
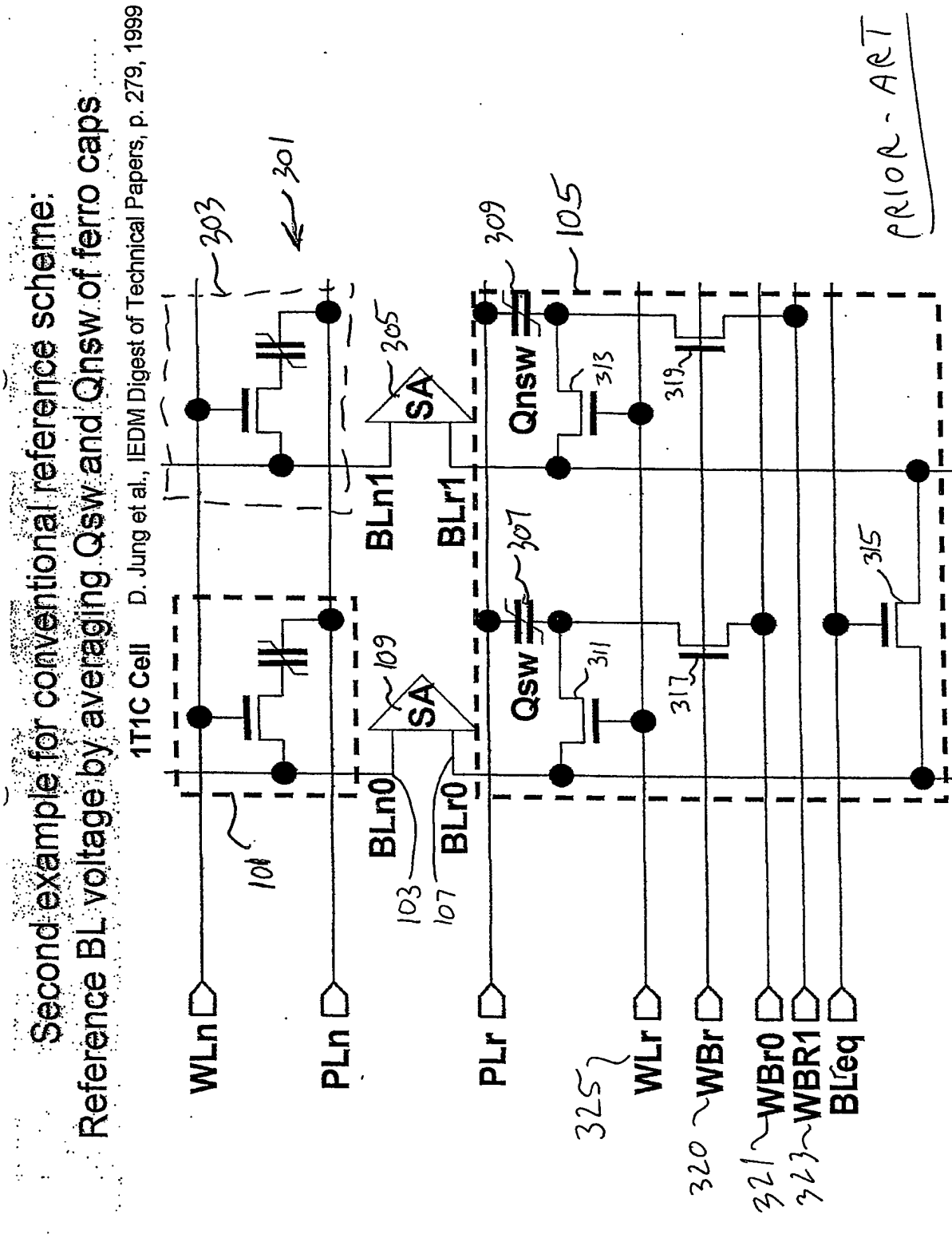
Conventional reference scheme:
Sense amplifier compares signals from 1T1C ferroelectric memory cell to a reference signal which is generated, e.g., by use of a non-switched ferroelectric reference capacitor/reference BL of appropriate area/capacitance or by averaging Qsw and Qnsw of two (or more) ferroelectric capacitors

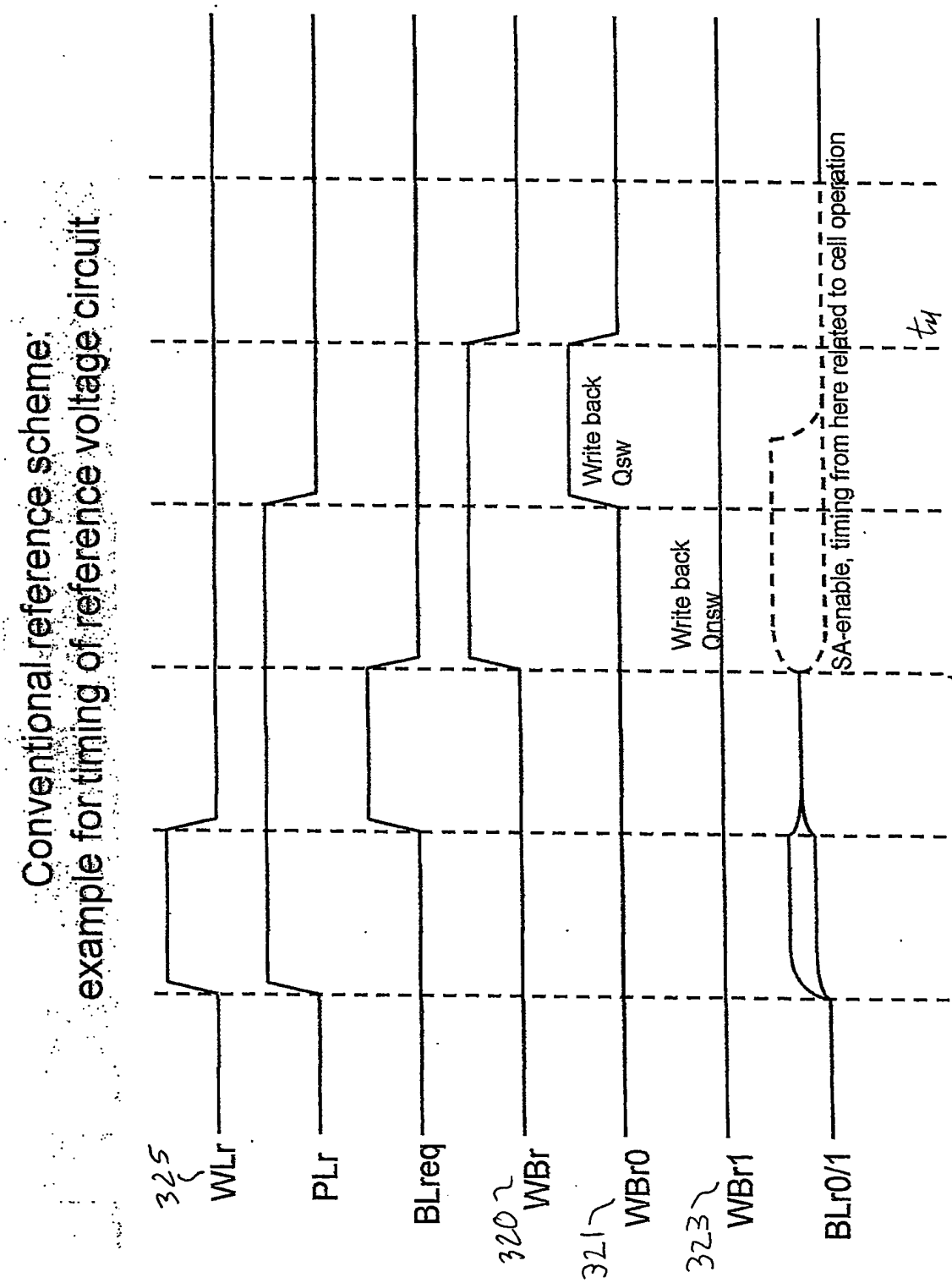


PRIOR - ART

Attachment to invention disclosure FDA I 03- 039

Fig. 1


Second example for conventional reference scheme:
Reference BL voltage by averaging Qsw and Qnsw of ferro caps
1T1C Cell D. Jung et al., IEDM Digest of Technical Papers, p. 279, 1999
WLn
PLn
PLr
WLr
WBr
WBr0
WBR1
BLeq
BLn0
BLr0
BLn1
BLr1
SA
SA
Qsw
Qnsw
101
103
107
109
301
303
305
307
309
311
313
315
317
319
320
321
323
325
105
Circuit for generation of reference voltage
Attachment to invention disclosure FDA I 03- 039
PRIOR - ART
FIG. 2



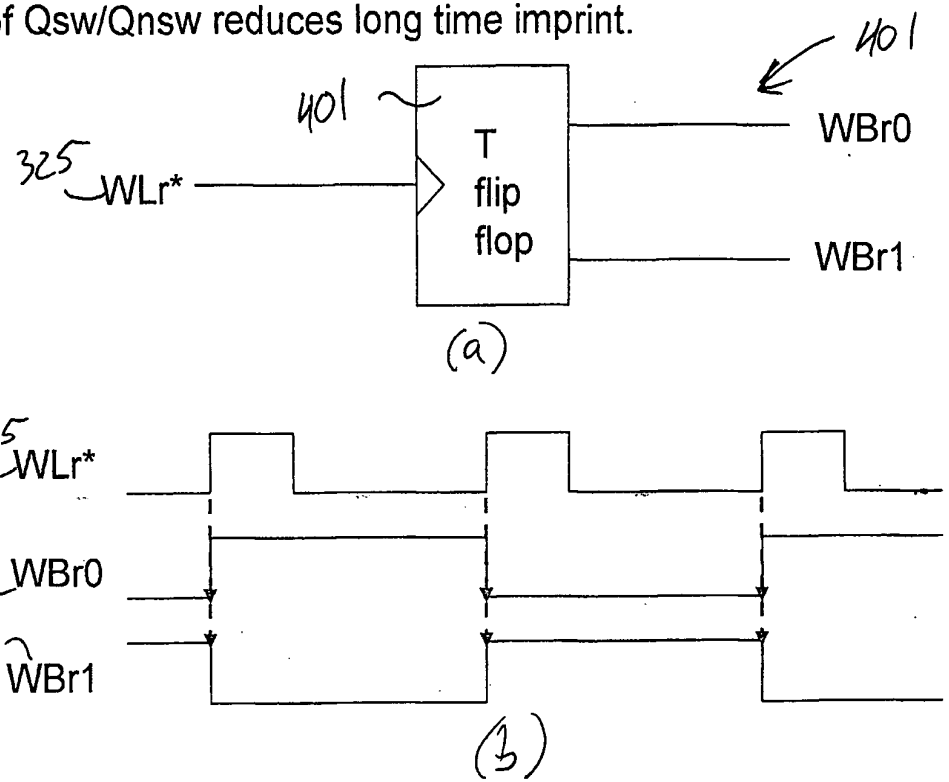
PRIOR-ART

FIG. 3

Attachment to invention disclosure FDA I 03-039

invention

Alternating with each access, Qsw and Qnsw are stored in the ferroelectric reference capacitors.
Background: Fatigue-free PZT is possible, but Imprint-free PZT not.
=> Toggling of Qsw/Qnsw reduces long time imprint.



* ~~Other signals can also be used as trigger s~~ignal

FIG. 4

Attachment to invention disclosure FDA I 03 - 038

invention: example for toggle flip flop

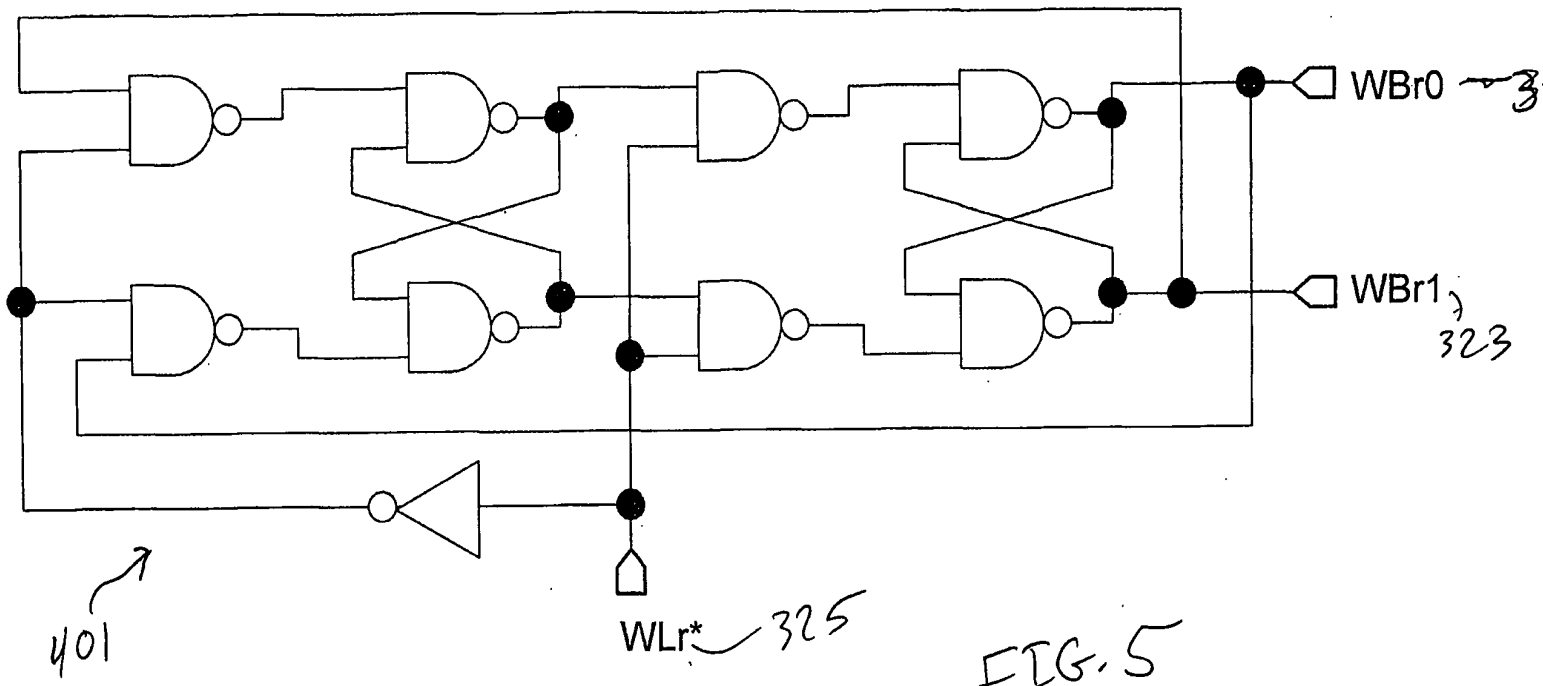


FIG. 5

* Other signals can also be used as trigger signal

Attachment to invention disclosure FDA I 03 - 038

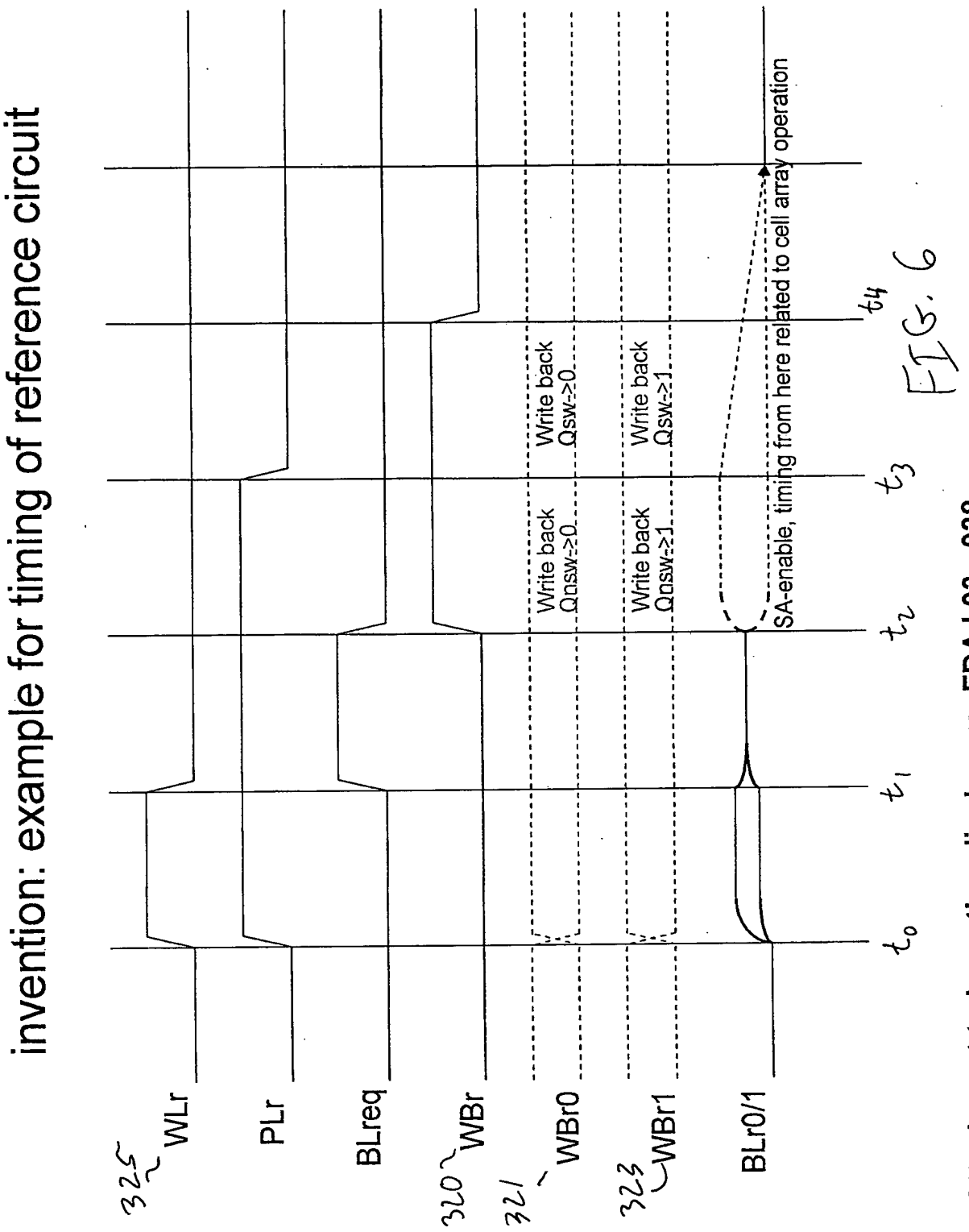


FIG. 6

Attachment to invention disclosure FDA I 03 - 038

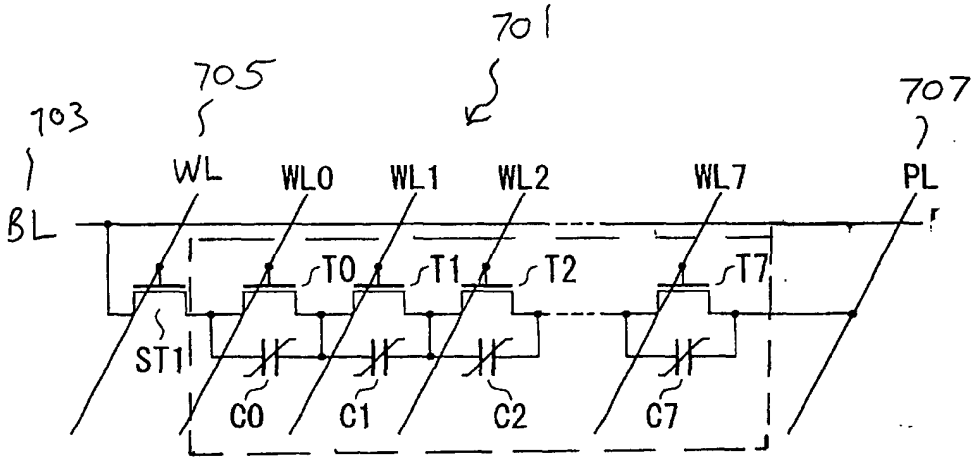


Fig. 7